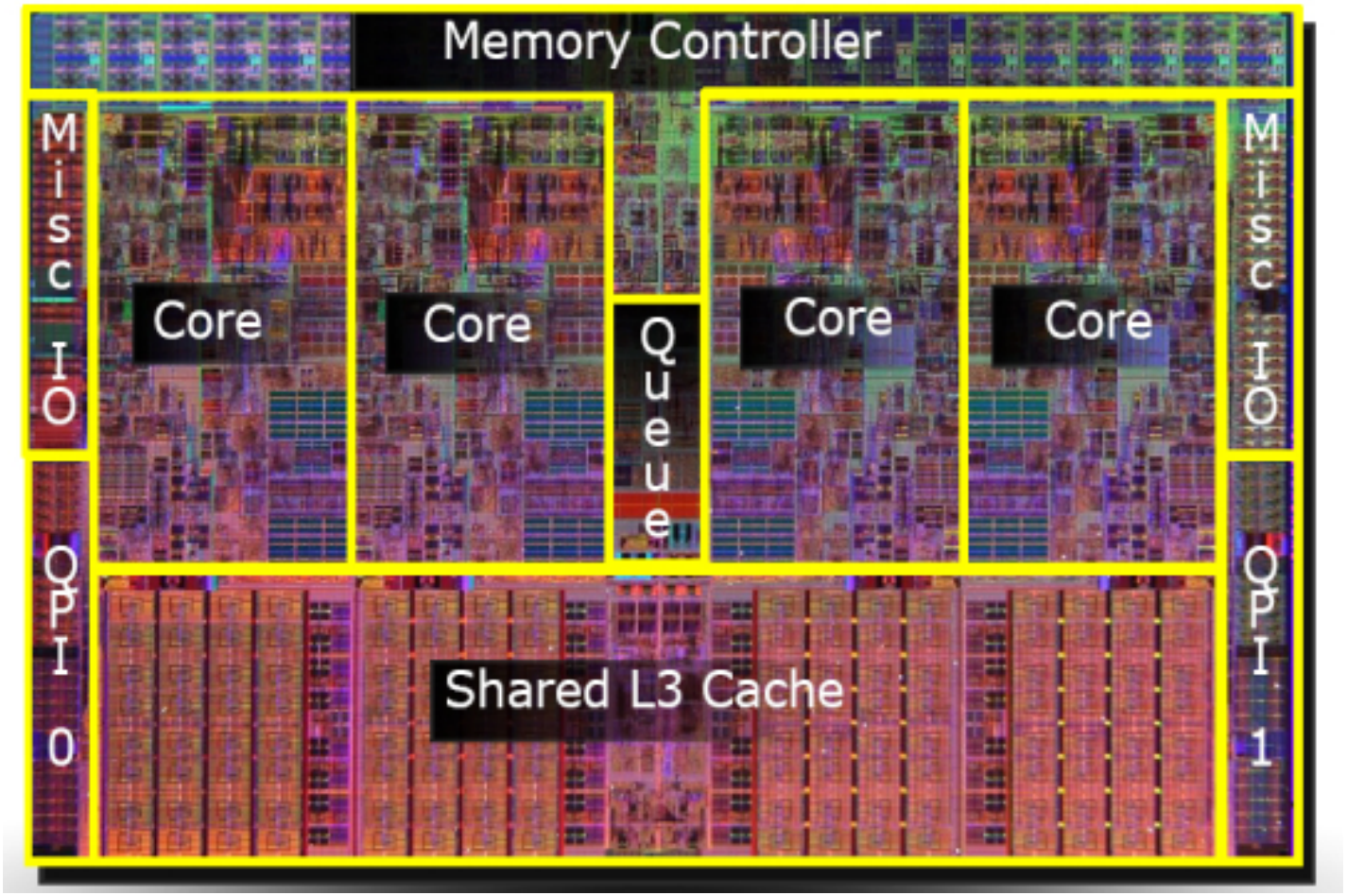
Non-Volatile Microprocessor Caches

Boon or Bane?

Sudhanva Gurumurthi

University of Virginia
Department of Computer Science

Cache Leakage Power is a Growing Problem!

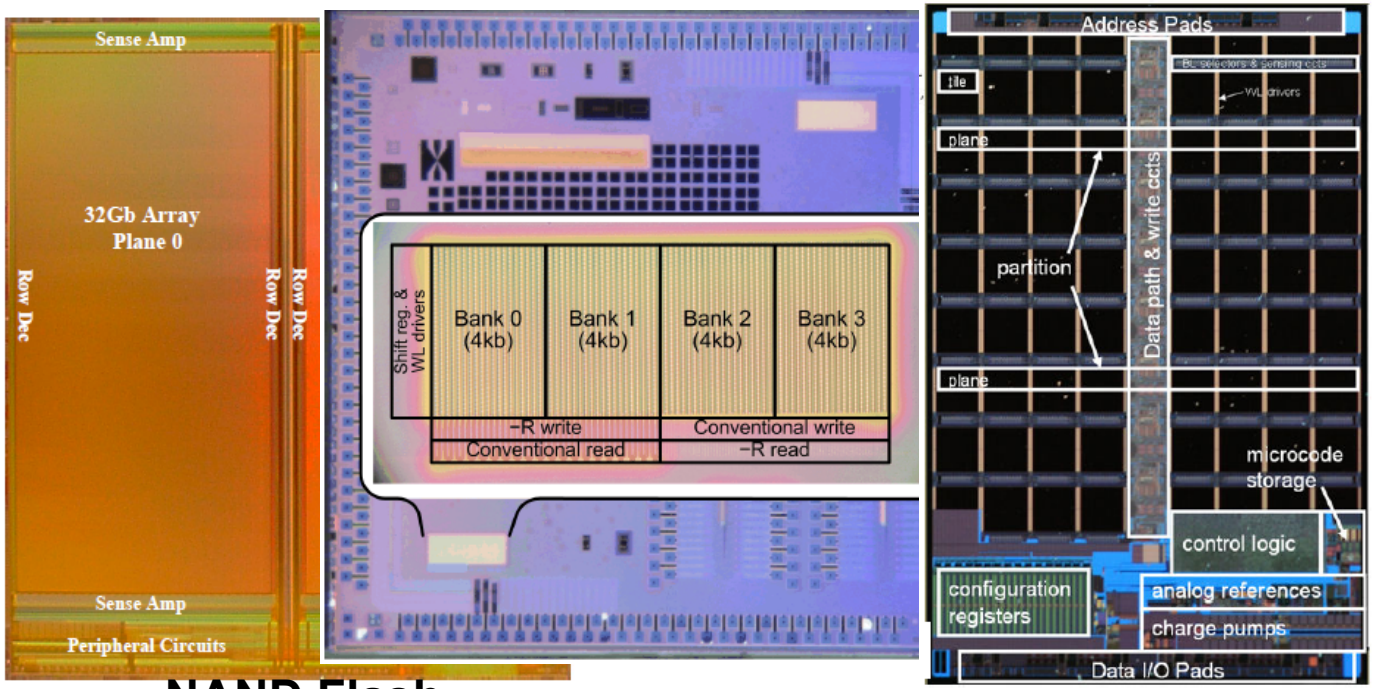


Intel Nehalem Die Photo Source: arstechnica.com

Non-Volatile Memory

Retain data for a long time without an external power source.

Little to no leakage in the memory cells



NAND Flash

Trinh et al., ISSCC 2009

Storage

Spin-Torque Transfer RAM (STT-RAM)

Halupka et al., ISSCC 2010

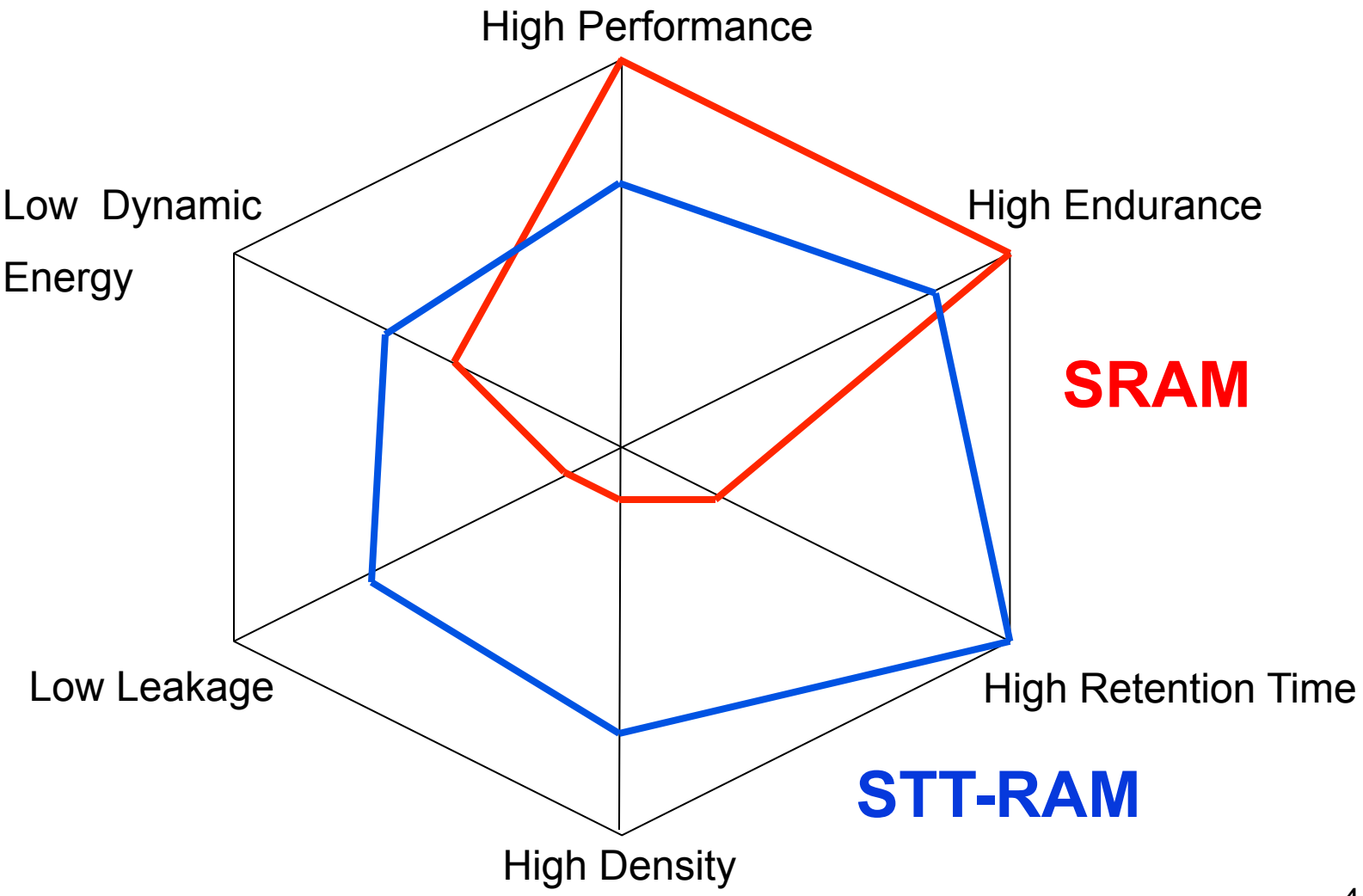
Caches

Phase Change Memory

Bedeschi et al., ISSCC 2008

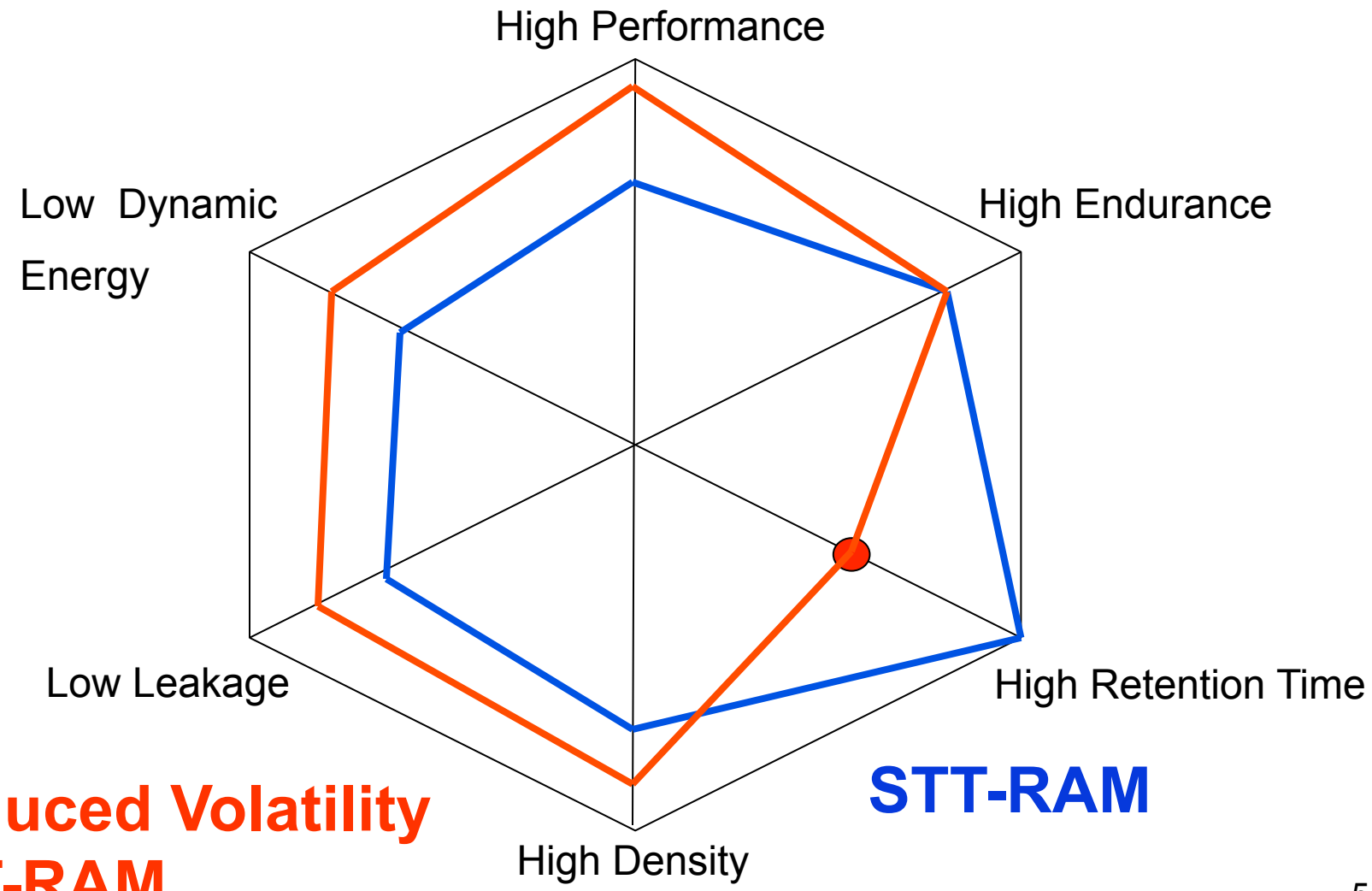
Main Memory

SRAM vs. STT-RAM



Relaxing Non-Volatility

[HPCA 2011, ISLPED 2011]

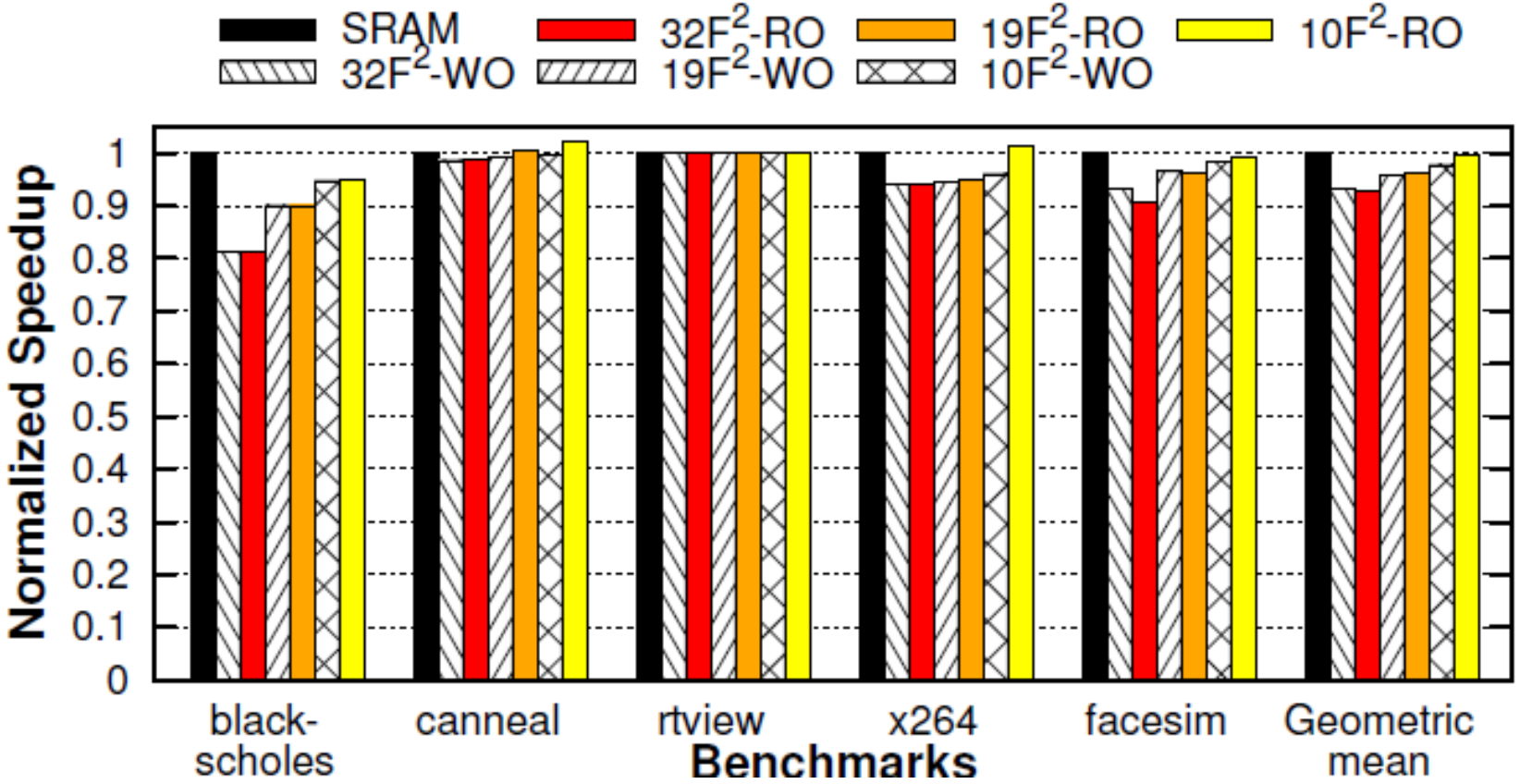


Reduced Volatility STT-RAM

- **Storage Class: 10 years**
- **Reduced Volatility: Seconds to Minutes**
- Actual retention times depend on the choice of memory cell geometry and operating temperature

SRAM vs. STT-RAM Cache Hierarchy

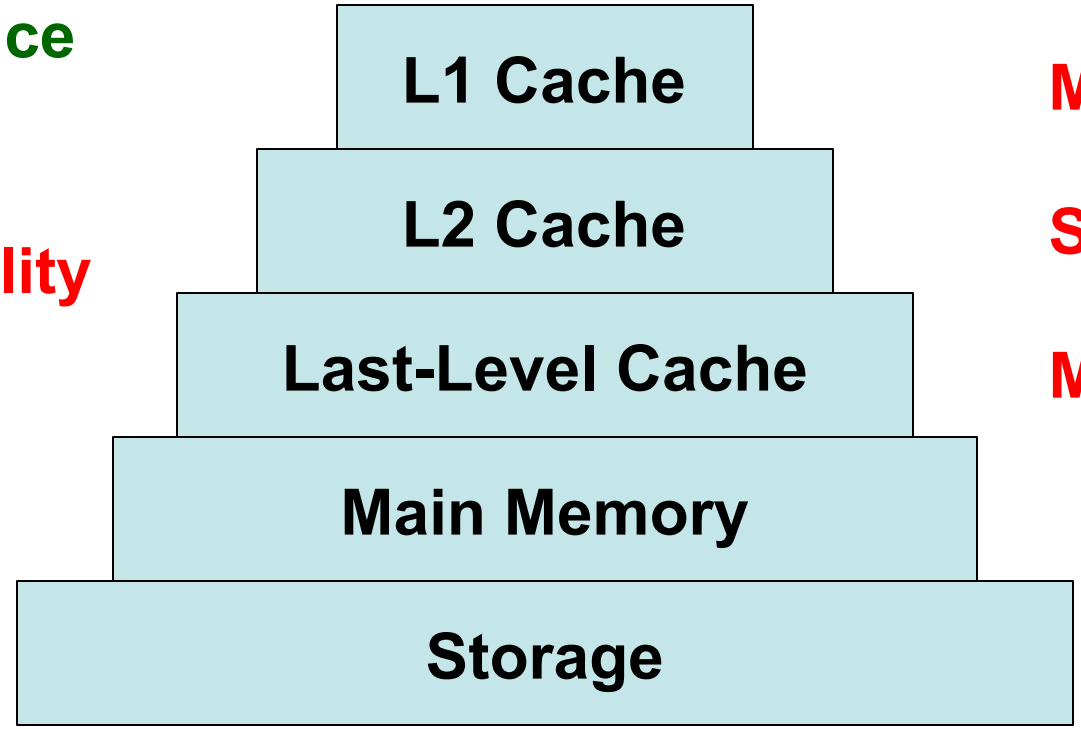
Performance Gap for 4-core processor



Avoid premature data loss using a cache line "refresh" mechanism.

Non-Volatility Close to the CPU

Cost
Performance
Capacity
Latency
Non-Volatility



"Degree" of Non-Volatility

Microseconds

Seconds

Minutes

What Impact Would Such a Cache Hierarchy Have On Transaction Systems?

Thank You

E-mail: gurumurthi@virginia.edu

UNIVERSITY of VIRGINIA
DEPARTMENT of COMPUTER SCIENCE